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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,218	11/20/2003	Wen-Chou Vincent Wang	ALTRP100/A1198	3208

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,218	WANG ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *01 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 37-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16 and 37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Therefore presently the earliest available filing date is the U.S filling date namely November 20, 2003.

Applicant's submission filed on June 01, 2006 has been entered.

Therefore , claim 1 as amended by the amendment and claims 2-16 and 37-40 as previously recited are pending in the Application.

Claims 17 to 36 have been cancelled .

Information Disclosure Statement

To date no IDS has been filed in this Application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 16 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiStefano (U.S. Patent No. 6,709, 895,herein after Distefano) previously applied

and further in view of Iijima (Japanese Published Patent Application No. P2003-030767 and the corresponding U.S. Printed Publication No. 2004/0155358, in the rejection below reference will be made to o U.S. publication only for the sake of English language).

With respect to claim 1 Tanaka describes a semiconductor package comprising: a die having a plurality of layers of low-K dielectric material in the die(Fig. 2# 61 chip/die, col. 3 line 24, # 2 low –k die electric material).

Tanaka does not specifically mention the layers of low-K dielectric material in the die .

However, Iijima in para 0008 describes (the well known in the art) of the layers of low-K dielectric material in the die/chip to provide dies/chips having high thermal resistance to withstand subsequent processing steps using lead free solder, etc. performed under high temperature conditions.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Iijima's chip/die having the layers of low-K dielectric material in the die instead of Tanak's die in Tanaka's device, the motivation to make the combination is to provide dies/chips having high thermal resistance to withstand subsequent processing steps using lead free solder, etc. performed under high temperature conditions. (iijima paras 0006 and 0007).

The remaining limitations of claim 1 are :

Distefano figure 7 # 132-die figure 1 # 32 die dielectric layers 20,26) the die having a top surface, a bottom surface, and a plurality of side surfaces, each surface having

associated corner and edge regions, (Distefano figures land 7, etc.) a wire bonding packaging substrate having a plurality of electrical contacts, (Distefano figure1 # 66, col. 1 line 61, figure 7 # 440) the packaging substrate being positioned under the die (Distefano fig.1 66 under 32, co1.8 lines 55-60, figure 7 shaded portion under 432) ; a plurality of interconnects electrically connecting the die to the plurality of electrical contacts, (DIstefano figure 1 54, col. 7 lines figure 7 # leads not numbered similar to flexible leads 54 in figure 3) a molding interface material applied to at least a portion of the top surface of the die, (Distefano figure 1 52 figure 7, col. 13 lines 55 to 65, Iijima figure1 #8 over 1 , para 0024 ,etc.) the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die; (Distefano figure 1 52 figure 7, col. 13 lines 55 to 65) and a molding cap covering at least a portion of the die, packaging substrate, interconnects, and molding interface material. (Distefano ,figure 1 58 figure 7 # 459). With respect to claim 2 Disteano describes a semiconductor package as recited in claim 1, wherein the molding interface material is configured to introduce compressive stress to the die, (it is inherent that the same material disclosed by Distefano as that claimed by Applicants' will recite the same compressive stress as claimed herein) thereby strengthening the die against the at least one of tensile and shear stresses. (it is further inherent that increase in one kind of stress (comrpesssive) will reduce the other (tensile and/or shear stress and strengthen the die against the at least one of tensile and shear stresses.

The recitation, 'wherein the molding interface material controls by applying compressive stress to the die, thereby strengthening the die against the at least one of

tensile and shear stresses" is taken to be a hybrid functional and product by process recitation for which patentable weight cannot be given.

With respect to claim 3 Distefano describes a semiconductor package as recited in claim 1, wherein the molding interface material is polyimide. (Distefano col. 8 lines 9 to 16).

With respect to claim 4 Di Stefano describes a semiconductor package as recited in claim 3, wherein the molding interface material is on at least a portion of the plurality of side surfaces of the die. (Di Stefano figure 7 encapsulant 458 on sides of 432).

With respect to claim 5 Di Stefano describes a semiconductor package as recited in claim 4, wherein the molding adjacent portion of the packaging interface material is also on a corresponding substrate in order to secure the die to the packaging substrate. (Distefano figures 1-7).

The limitation " in order to secure " is also taken to be a product by process limitation for which no patentable weight can be given. See discussion above under claim 2 (incorporated here by reference).

With respect to claim 6 Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material covers multiple non-contiguous regions to the top surface of the die. (Distafano figures1- 7).

With respect to claim 7 Di Stefano describes a semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is rectangular in shape. (Distafano figures 1- 7)

With respect to claim 8 Di Stefano describes a semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is triangular in shape. (Distafano figures1-7)

With respect to claims 9 Di Stefano describes a semiconductor package as recited in claim 6, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns. (Claim 9 depends from claim 6 and the product by process limitation not being given patentable weight in claim 6 is also applicable here.).

With respect to claims 10 and 12, 11Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material is a contiguous region on the top surface of the die excluding corner regions. (Distafano figure 7)

With respect to claim 1 1 Di Stefano describes a semiconductor package as recited in claim 10, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns. (DiStefano figures, entire patent) With respect to claim 13 Di Stefano describes a semiconductor package

as recited in claim 12, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns. (rejected for same reasons as claim 11)

With respect to claim 14 Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material has a coefficient of thermal expansion between 5 ppm and 40 ppm. (Distefano col. 8 lines 17-40, col. 9 lines 18 to 65).

With respect to claim 15 Di Stefano describes a semiconductor package as recited in claim 14, wherein the molding interface material is over a substantial portion of the die such that a stress buffer zone is established between the die and the molding cap. (DiStefano figures 1- 7, col. 13 lines 53-62).

With respect to claim 16 Di Stefano describes a semiconductor package as recited in claim 1, wherein the plurality of layers includes extra low-K dielectric material. (Di Stefano col. 6 line 3 polyimide known in the art to be low k-dielectric material).

With respect to claim 37 DiStefano describes a Semiconductor package as recited in claim I where the molding interface material is a layer positioned between and in contact with the die and the molding cap. (Distefano 52 between 32 and 58 figures)

With respect to claim 38 DiStefano describes a semiconductor package as recited in claim 1 wherein the plurality of low-K dielectric material has a CTE between the range of 20 ppm and 50 ppm. (Distefano col. 8 lines 17-40, col. 9 lines 18 to 65).

With respect to claim 39 Di Stefano describes a semiconductor package as recited in claim 38, wherein the plurality of low-K dielectric material has a dielectric constant between 2.6 and 3.5. (polyimide dielectric constant between 3.1-3.4, and other materials described in DiStefano)

With respect to claim 40 DiStefano describes a semiconductor package as recited in claim 38, wherein the plurality of low- K dielectric material has a dielectric constant between 2.2 and 2.6. (DiStefano col. 7 line 51 to col. 8 line 16).

Response to Arguments

Applicant's arguments with respect to claims 1 to 16 and 37 to 40 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven H. Rao

Patent Examiner

December 10, 2006.